HIGH-SPEED QPSK MODULATOR AND DEMODULATOR WITH SUBHARMONIC PUMPING

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ABSTRACT

A high-speed QPSK modulator and demodulator are described. Both units are pumped with a common 6.5 GHz local oscillator giving a modulated carrier at 13 GHz. Data can be transmitted and recovered at speeds up to a total information rate of 3.6 Gbit/s with errors less than 10^{-11}.

INTRODUCTION

A new type of high-speed QPSK modulator/demodulator has been devised for use in digital communication links operating at gigabit per second transmission rates. Inherent in the modulator is the multiplexing of two baseband data streams each having bit rates up to half the maximum information rate. The basic modulator circuit can also demodulate and demultiplex the QPSK signal into the component bit streams entering the modulator. The microwave circuitry is broadband, and the frequency range of operation is determined primarily by the local oscillator circuit which operates at one half of the carrier frequency. The frequency band can be shifted by scaling circuit dimensions and local oscillator frequency with a proportionate scaling of the maximum information rate within limits imposed by parasitics in the nonlinear modulating elements.

Modulators which operate at high data rates and frequencies have been reviewed in detail by Cuccia and Mathews [1]. These circuits employ well known digital modulation schemes treated by Sinnema [2], Greenstein and Fitzgerald [3], and Leuenberger [4], [5]. A major difficulty in realizing QPSK modulators at gigabit data rates is multiplexing the bit streams and local oscillator frequency with low leakage to the output port. We show that this can be achieved with microstrip and finline components on a single substrate with subharmonic pumping. We also demonstrate that the bit error rates of the new modulator circuit are less than 10^{-11} which makes it suitable for use in digital communication links.

A prototype modulator-demodulator pair has been constructed for a carrier frequency of 13 GHz with a maximum design information rate of 2 Gbit/s. The performance of each unit has been evaluated and adjusted to give satisfactory performance with a single tuning element in the local oscillator circuits. Bit error rates were measured for transmission of pseudo-random data streams through the modulator-demodulator pair.

THEORY OF OPERATION

A simplified schematic of the modulator is shown in Fig. 1. Two NRZ bit streams enter the modulator in the in-phase *(I)* and quadrature *(Q)* ports. Each of these baseband signals has two states with the same amplitudes but with opposite polarities. The mixing elements have anti-symmetrical nonlinear characteristics which are realized by pairs of paralleled opposed Schottky diodes. Mixing of a data stream with the local oscillator signal produces second harmonic components of the local oscillator frequency with a 180° phase difference corresponding to the bit polarities in the data stream. A 45° phase difference in local oscillator signals at each modulating element gives second harmonics in quadrature for the two modulators. Summation of the local oscillator second harmonics from each modulator element results in a QPSK modulated signal centered at twice the local oscillator frequency. Since each of the four phase states is the vector sum of two signals, each coming from the in-phase and the quadrature mixers, inequalities in the amplitudes of these signals will lead to phase errors in the resultant output components. Similarly deviation in the phase difference from $\pi/4$ between the local oscillator signals injected into the two mixers will cause differing amplitudes of the output components.

The modulator in Fig. 1 can also operate as a QPSK demodulator as shown in Fig. 2. Modulated signals entering the splitter are separated into two equal components and mix with the two subharmonic local oscillator components offset in phase from one another to produce baseband NRZ bit streams. The local oscillator phase angle θ is adjusted to give the appropriate baseband bit streams out of the I and Q ports. This implies phase coherence between the local oscillators for both the modulator and demodulator.

As in the modulator, non-ideal components in the demodulator introduce distortions in the output bit streams. Unequal splitting of the signal at the input of the demodulator or different conversion losses in the two mixers give unequal amplitudes at the I and Q ports. If the phase difference between the local oscillator signals injected into the I and Q mixers is not $\pi/4$, both bit streams cannot be recovered without some crosstalk. It is possible to remove or reduce these distortions by processing the emergent bit streams.

CIRCUIT REALIZATION

The QPSK modulator shown schematically in Fig. 1 is built on a dielectric substrate which has etched conductor patterns on both the top and the bottom surface. The substrate, RT/Duroid 5880, has a relative dielectric constant of 2.20, a thickness of 0.031" and an electrodeposited copper cladding (1 ounce/ sq.ft.). The substrate is inserted into an aluminum housing which has two coaxial connector inputs for the incoming bit streams, a rectangular waveguide input port for the local oscillator at 6.5 GHz, and a coaxial output for the modulated 13 GHz carrier.

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Conductor patterns are shown in Fig. 3. (In Fig. 3a the dark areas are metalized, but in Fig. 3b the metal coating is removed.) The incoming data streams are first transmitted through two low-pass filters with a cutoff frequency of 2 GHz. These five-section L-C microstrip filters are needed to prevent the 6.5 GHz local oscillator power from reaching the input ports of the data streams. The local oscillator input is shown at the bottom of Fig. 3a. The waveguide mode at the input is transformed to a finline mode by means of a stepped impedance transformer. A finline power divider is used to transmit half the pump power to each mixer circuit. The finline sections are etched into the ground plane of the Duroid substrate. In order to achieve the required phase shift of $\pi/4$ shown in Fig. 1 in one arm of the pump circuit it is necessary that the lengths of the finline sections after the power divider are different. The lengths of the horizontal finline sections shown in Fig. 3b differ by one eight wavelength in the finline. The local oscillator power traveling in the horizontal sections of the finlines of Fig. 3b is coupled to the microstrip lines by means of finline-to-microstrip couplers.

Both data streams and the pump power are transmitted through low-pass filters to the mixer diodes for upconversion to a 13 GHz carrier. The cutoff frequency of each low-pass filter is 6.6 GHz which permits transmission of the pump but rejects the upconverted and modulated carrier at 13 GHz. The frequency conversion is performed with commercially available beam-leaded Schottky diodes (HP types HSCH-5311 and HSCH-5510) which are connected in anti-parallel. A high-pass filter with a cutoff frequency of 9.3 GHz transmits the modulated carrier and provides the *dc* return for the bit streams. The filter is grounded to the sidewall via a microstrip-to-antipodal finline transition which has a low transmission loss at the carrier frequency and reflects the pump frequency. The modulated carriers are subsequently added in a Wilkinson power adder, and the sum appears at the output terminal of Fig. 3.

PERFORMANCE

Phase and magnitude of the modulator output were measured with *dc* signals on the I and Q ports to verify operation of the device. For best operating conditions the output power was approximately -10 to -13 dBm with ± 0.2 V dc signals input and 10 mW local oscillator power. The test arrangement in Fig. 4 was used to measure both relative phase and amplitude.

Modulator circuits were operated as demodulators and were tested for orthogonality of the output at the I and Q ports as shown in Fig. 5. The modulator in Fig. 5 operates as a frequency doubler whose phase is varied with the phase shifter, The I and Q output voltages are sinusoidal functions of the phase angle.

Bit error rates were measured for data bit streams as high as 2 Gbit/s passing through a modulator-demodulator pair as shown in Fig. 6. Two bit streams for the I and Q inputs were obtained by splitting the output stream from the generator into two parts, one of which was delayed with respect to the other. The line stretcher adjusted the phase between the modulator and demodulator and was set for minimum cross coupling between I and Q output signals from the demodulator.

Data trains and eye diagrams of the modulator-demodulator pair outputs are shown in Fig. 7 with 50 Mbit/s pseudo-random input data streams. Some cross talk is evident by sharp pulses in each data train when the state of the other train changes. Eye diagrams in Fig. 7 are open, and transitions are well defined with bit error rates lower than 10^{-11}. Eye diagrams in Fig. 8 are relatively clean up to 1.5 Gbit/s but are quite diffuse at 2 Gbit/s. Error rates are smaller than 10^{-11} up through 1.5 Gbit/s rising to 5×10^{-3} at 2 Gbit/s. The low-pass filters on the I and Q ports cut off at 1.9 GHz causing the degradation in performance at 2 Gbit/s.

CONCLUSIONS

A QPSK modulator operating at a 13 GHz carrier frequency which is subharmonically pumped has been built. This modulator can also be operated as a demodulator. Typical operating conditions and bit error rates for the combination are summarized:

13 GHz QPSK MODULATOR - DEMODULATOR	
OPERATING CONDITIONS	
Bit Rate/Rail	0 - 2 Gbit/s
Bit Stream Input Levels	± 90 mV
Bit Stream Output Levels	± 11 mV
Carrier Frequency	12.9 GHz
Local Oscillator	
Frequency	6.45 GHz
Power (Modulator)	4 dBm
(Demodulator)	4 dBm
BIT ERROR RATES/RAIL	
50 - 1500 Mbit/s:	$< 10^{-11}$
2000 Mbit/s:	$\leq 5*10^{-3}$

The modulator-demodulator pair can transmit at information rates to 1.8 Gbit/s for each rail with low error rates. corresponding to a total information rate of 3.6 Gbit/s.

REFERENCES

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[4] K. J. Leuenberger, "Digital Radio Systems Examined - Part I, General State of the Art," MSN & Communications Technology, vol. 16, pp. 81-92, Jan. 1986.

[5] K. J. Leuenberger, "Digital Radio Systems Examined - Part II, Modulation and Transmission Characteristics," MSN & Communications Technology, vol. 16, pp. 131-143, Feb. 1986.

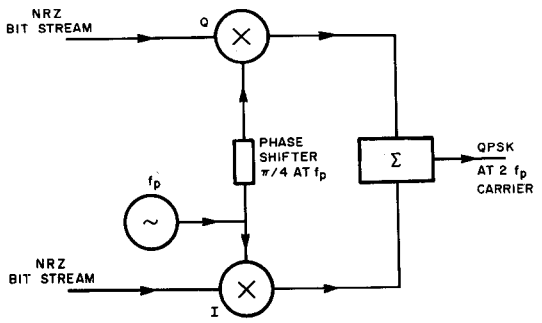

Fig. 1 Schematic diagram of subharmonically pumped QPSK modulator.

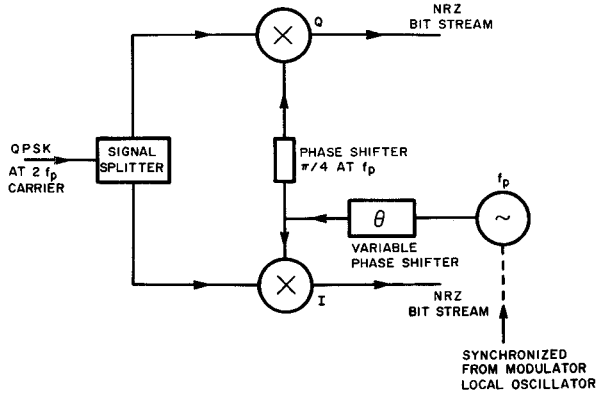

Fig. 2 Schematic diagram of QPSK modulator operated as a demodulator.

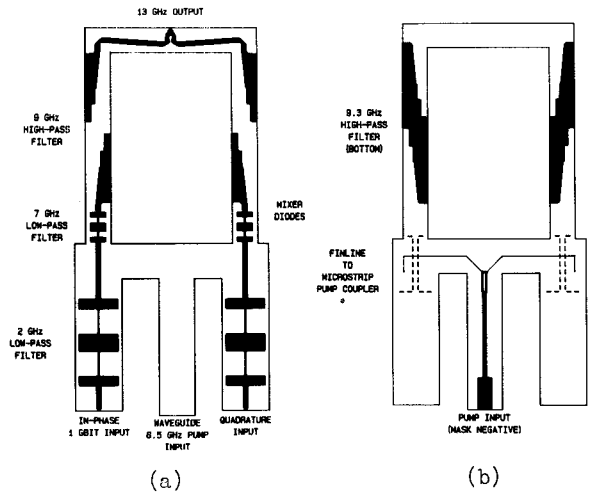

Fig. 3 Mask patterns for the two sides of the Duroid substrate. Details of the microstrip components are shown in (a) with finline details in (b). Note that metalization is present in dark areas of (a) but has been removed in the dark area of (b).

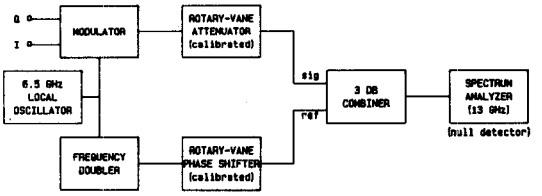

Fig. 4 Bridge to measure phase and amplitude of modulator output for each of the four modulator states.

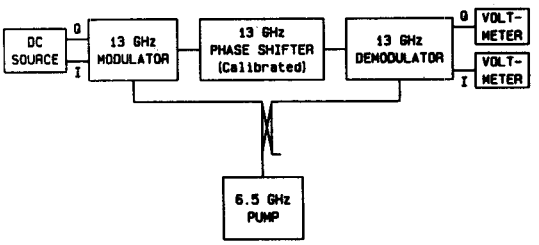

Fig. 5 Arrangement for testing performance of the demodulatior for static data states. Voltmeter readings are sinusoidal with the phase angle setting at 13 GHz and in quadrature with each other.

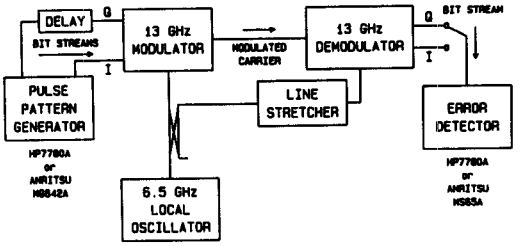

Fig. 6 Bit error rate test set.

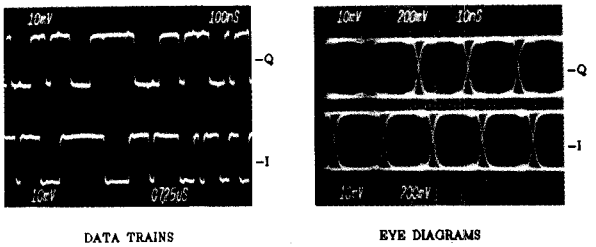

Fig. 7 Recovered data trains and eye diagrams at 50 Mbit/s.

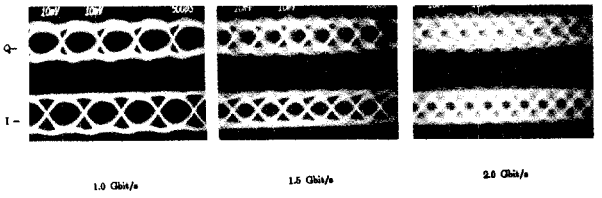

Fig. 8 Output eye diagram for recovered data trains from 1 to 2 Gbit/s on each rail.